METHOD FOR ETCHING A METAL LAYER IN A SEMICONDUCTOR DEVICE

Field of the Invention

The present invention relates to a method for forming metal lines in a semiconductor device; and, more particularly, to a method for simultaneously etching a metal layer throughout the entire surface of a wafer or substrate without causing microloading.

Background of the Invention

Recently, as a semiconductor device becomes highly integrated, in a process for fabricating a semiconductor device, metal lines of about 0.25 ㎛ or smaller in width are required. As a result, it is general to use a DUV (Deep Ultra Violet) photoresist film in forming the metal lines.

As the photoresist film is sensitive to a reflectance of the metal lines, the reflectance should be decreased to form a non-defective photoresist pattern. For the reason, an oxide-based antireflective coating ("ARC") layer coated on the metal lines is widely used.

However, when an in-situ etching process of the ARC layer is performed in a metal etching chamber, functions of the device may be deteriorated due to a microloading effect between a center area and an edge area of a wafer or

substrate. The microloading effect becomes more serious in a far edge area being away from the center area.

As an approach for decreasing the microloading effect, there has been proposed a process for improving a uniformity of metal lines. However, such a process has a limitation in overcoming a difference in etching rate between areas of the wafer. The problem is closely related with a deposition of polymers in the chamber. Especially, when a Si-X based ARC material is deposited in the chamber, such phenomenon becomes more severe.

Figs. 1A and 1B illustrate cross sectional views showing states after etching of an ARC layer 2 and after etching of metal layers 3 and 5, respectively.

As shown in Fig. 1A, in etching the ARC layer 2, the metal layer 3 in a center area of a wafer 4 is exposed earlier than in an edge area of the wafer since the etching rate is higher at the center area than at the edge area.

Also, referring to Fig. 1B, after etching of the metal layer 3, the TiN layer 5 in the edge area is exposed less than in the center area.

That is, in such a conventional process, the etching rate of the ARC layer is greater in the center area than in the edge area so that the metal layer may be excessively etched and there may occur an underetch in the edge area.

When comparing the etching rates in the far edge area and the center area on the basis of a 10 ㎜ wafer edge

exclusion, experimental results indicate that the etching rate difference between the edge area and the center area is 1400 Å/min or more.

Summary of the Invention

It is, therefore, an object of the present invention to provide a method for simultaneously etching a metal layer wherein an etching rate decrease in an edge area of a wafer is prevented by performing an additional dry cleaning process using a fluorine-based gas to eliminate a Si-X based polymer deposited in a chamber, thereby minimizing a microloading effect.

In accordance with a preferred embodiment of the present invention, there is provided a method for etching a metal layer on which an oxide-based ARC layer is coated in a semiconductor device comprising the step of:

performing a dry cleaning process by using a Cl_2/CHF_3 based gas, after dry cleaning the ARC layer by using an oxide-based gas.

Brief Description of the Drawings

The above and other objects and features of the present invention will become apparent from the following description of preferred embodiments, given in conjunction

with the accompanying drawings, in which;

Figs. 1A and 1B illustrate cross sectional views sequentially showing a conventional process of etching a metal layer;

Figs. 2A and 2B depict cross sectional views sequentially showing a process of etching a metal layer in accordance with a preferred embodiment of the present invention; and

Fig. 3 shows a graph of an etching rate comparison between the conventional method and the present invention.

Detailed Description of the Preferred Embodiments

A preferred embodiment of the present invention will now be described in detail with reference to the accompanying drawings, wherein like reference numerals appearing in the drawings represent like parts.

Figs. 2A and 2B illustrate cross sectional views showing an etching process of an ARC layer 2 and an etching process of metal layers in accordance with the preferred embodiment of the present invention, respectively.

As shown in Fig. 2A, after the ARC layer 2 has been etched, there is substantially no difference between the etching depths in a center area and an edge area of a wafer 4.

As a result, as shown in Fig. 2B, the metal layers 3

and 5 in the center area and the edge area can simultaneously be etched.

This process is carried out by using two steps as indicated in Table 1.

Table 1

	Pressure (mTorr)	Source power(W)	Bias power(W)	O_2 (sccm)	Cl_2 (sccm)	CHF_3 (sccm)
First step	8 ~ 50	500 ~ 1200	0 ~ 10	300 ~ 500	0	0
Second step	8 ~ 50	500 ~ 1200	0 ~ 10	0	100 ~ 200	5 ~ 30

* sccm : Standard Cubic Centimeter per Minute

As in the second step of Table 1, in order to eliminate polymers, e.g., $AlCl_x$ and Si-X, which are byproducts deposited in a metal etching chamber, a Cl_2/CHF_3 based dry cleaning process is employed; and, therefore, the process results as shown in Figs. 2A and 2B are obtained.

At this time, the process is preferably performed for about 5 seconds to about 30 seconds.

Fig. 3 shows a graph of an etching rate comparison between a conventional process and the process of the present invention.

As shown in Fig. 3, because a microloading effect of the etching rate in the present invention is less than that

of the conventional method, the etching rates of the center area and the edge area are substantially same.

Here, in the edge area, the data of Fig. 3 were obtained on the basis of a 10 ㎜ wafer-edge exclusion.

In accordance with the present invention, the etching rate in the edge area is not decreased, because the etching process at the edge area is not hindered.

Experimentally, when comparing the etching rates in the center area and the far edge area on the basis of the 10 ㎜ wafer-edge exclusion, there is substantially no difference therebetween, thereby preventing the underetch which may occur in the far edge area.

As a result, the reliability of the metal etching process is improved, and in the etching process of the metal layers 3 and 5 having the ARC layer 2 thereon, a seasoning effect which may occur by a dry cleaning is reduced.

While the invention has been shown and described with respect to the preferred embodiments, it will be understood by those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the invention as defined in the following claims.